PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants: Jin Kook Jung et al.

Examiner: Sandvik, Benjamin P

Serial No: 10/822,384

Group: Art Unit 2826

Filed: April 12, 2004

Docket: 8021-224 (SS-19575-US)

For: SEMICONDUCTOR DEVICE AND METHOD OF LOCATING A PREDETERMINED POINT ON THE SEMICONDUCTOR DEVICE

APPEAL BRIEF

Appeal from Group 2826

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I. INTRODUCTION

This Appeal is from a Final Office Action mailed on October 11, 2007 finally rejecting claims 1-4, 23 and 24 of the above-identified application. Applicants commenced this Appeal by a Notice of Appeal dated December 11, 2007, which was filed with a Pre-Appeal Brief Request For Review. A Notice of Panel Decision from Pre-Appeal Brief Review dated January 22, 2008 states that the application remains under appeal because there is at least one actual issue for appeal. Accordingly, Applicants hereby submit this Appeal Brief.

II. REAL PARTY IN INTEREST

The real party in interest for the above-identified application is Samsung Electronics Co., Ltd., the assignee of the entire right, title and interest in and to the subject application by virtue of an assignment of recorded in the U.S. Patent and Trademark Office at reel 015204 frame 0728.

III. RELATED APPEALS AND INTERFERENCES

There are no Appeals or Interferences known to Applicants, Applicants' representatives or the Assignee, which would directly affect or be indirectly affected by or have a bearing on the Board's decision in the pending Appeal.

IV. STATUS OF CLAIMS

Claims 1-4, 23 and 24 are pending, stand rejected and are under appeal. The claims on appeal are set forth in the attached Appendix.

Claims 1, 23 and 24 are the only independent claims. Claims 2, 3 and 4 are directly depend from claim 1.

V. STATUS OF AMENDMENTS

An Amendment and Response to a Non-final Office Action dated June 25, 2007 was filed on September 21, 2007, and was entered.

VI. SUMMARY OF THE CLAIMED SUBJECT MATTER

In general, the claimed subject matter relates to marking patterns formed among dummy patterns of a semiconductor device to enable easy location of a point on the semiconductor device.

A. Embodiments Of Claims 1, 23 and 24

Claim 1 recites, inter alia, that a number of the dummy patterns is substantially greater than a number of the marking patterns.

For purposes of illustration, the embodiment of claim 1 will be discussed hereafter with reference to Figure 4 and the descriptions in Applicants' specification at page 7, line 5 – page 8, line 17. It is to be understood that the following description of the claimed embodiments and reference to the drawings are for illustrative purposes to provide some context for the claimed embodiments, but nothing herein shall be construed as placing any limitation on the claimed embodiments.

More specifically, by way of example, Applicants recognize that the marking patterns 115 are formed at intervals of 3 dummy patterns (110), however the length of the intervals can be any number of dummy patterns (110) deemed appropriate. Thus, when attempting to locate a desired

point on the semiconductor device, the marking patterns can be counted instead of individual dummy patterns (110). This makes locating the desired point easier and more reliable than the conventional method of counting individual dummy patterns (110). See, e.g., Applicants' disclosure, page 8, lines 5-11; Fig. 4.

As such, small numbers of marking patterns (115) are used to form a demarcation of larger numbers of dummy patterns (110).

Claim 23 recites, inter alia, that the marking patterns surround at least a group of dummy patterns, wherein a size of the marking patterns is smaller than a size of the dummy patterns.

For purposes of illustration, the embodiment of claim 23 will be discussed hereafter with reference to Figure 5 and the descriptions in Applicants' specification at page 8, line 18 – page 9, line 9. It is to be understood that the following description of the claimed embodiments and reference to the drawings are for illustrative purposes to provide some context for the claimed embodiments, but nothing herein shall be construed as placing any limitation on the claimed embodiments.

More specifically, by way of example, Applicants recognize that the marking lines (220) may be formed of marking patterns (215) that have a different size and/or shape from the dummy patterns (210) and surround blocks of the dummy patterns (210). In Fig. 5, the marking patterns (215) are smaller than, but the same shape as, the dummy patterns (210). See, e.g., Applicants' disclosure, page 9, lines 3-6; Fig. 5.

As such, the marking patterns (215) surround at least a group of dummy patterns (210), wherein a size of the marking patterns (215) is smaller than a size of the dummy patterns (210).

Claim 24 recites, inter alia, that the marking patterns and the predetermined plural numbers

of the dummy patterns grouped by the marking patterns form a unit, which is repeated.

For purposes of illustration, the embodiment of claim 24 will be discussed hereafter with reference to Figure 6 and the descriptions in Applicants' specification at page 9, line 10 – 19. It is to be understood that the following description of the claimed embodiments and reference to the drawings are for illustrative purposes to provide some context for the claimed embodiments, but nothing herein shall be construed as placing any limitation on the claimed embodiments.

More specifically, by way of example, Applicants recognize that marking lines (320) formed of marking patterns (315) that have a different size and/or shape from dummy patterns (310) are provided in the shape of a grid. In Fig. 6, the marking lines (320) demarcate 3x3 blocks of dummy patterns (310). See, e.g., Applicants' disclosure, page 9, lines 10-19; Fig. 6.

As such, the marking patterns (315) and the predetermined plural numbers of the dummy patterns (310) grouped by the marking patterns (315) form a unit (i.e., 3x3 blocks of dummy patterns (310)), which is repeated.

B. Embodiments Of Claims 2-4

Claim 2 recites, inter alia, that the marking patterns have a different shape from the dummy patterns. Claim 3 recites, inter alia, that the marking patterns have a different size from the dummy patterns. Claim 4 recites, inter alia, the marking patterns are smaller than the dummy patterns.

For purposes of illustration, the embodiments of claims 2, 3 and 4 will be discussed hereafter with reference to Figure 4, and the descriptions in Applicants' specification at page 7, line 18 to page 8, line 2. It is to be understood that the following description of the claimed embodiments and reference to the drawings are for illustrative purposes to provide some context

for the claimed embodiments, but nothing herein shall be construed as placing any limitation on the claimed embodiments.

More specifically, by way of example, as stated above, Applicants recognize that the marking patterns (115) are formed to be different from the dummy patterns (110) in terms of size and/or shape, so as to distinguish the marking patterns (115) from the dummy patterns (110). In the present embodiment of the invention, the marking patterns (115) are formed to be smaller than the dummy patterns (110). See, e.g., Applicants' disclosure, page 7, line 18 to page 8, line 2.

VII. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4, 23 and 24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication No. 2002/0175419 ("Wang").

VIII. ARGUMENT

A. Rejections Of Claims 1-4, 23 and 24 Under 35 U.S.C. § 102

In rejecting claims under 35 U.S.C. 102, the Examiner must show that the reference teaches every element of the claims. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

1. The Rejections Of Independent Claims 1, 23 And 24 Are Clearly Erroneous

a. The Examiner has failed to show that Wang discloses a number of the dummy patterns substantially greater than a number of the marking patterns as claimed in claim 1

In the October 11, 2007 Final Office Action, the Examiner states that Wang teaches dummy patterns (700) and marking patterns (1200) wherein a number of the dummy patterns (700) is substantially greater than a number of the marking patterns (1200). See October 11, 2007 Final Office Action, Page 2. In stark contrast to the Examiner's assertion, elements (1200) are not marking patterns, but vias. The vias form plugs when filled with a metal layer in a subsequent process. See e.g., paragraph [0075] of Wang. As such, the vias (1200) cannot be marking patterns used for counting the dummy patterns because the vias (1200) are hidden when filled with the metal layer.

Furthermore, Wang does not disclose that a number of the dummy patterns is substantially greater than a number of the marking patterns. If the vias (1200) in Fig. 12B, assuming *arguendo*, were marking patterns, other vias (602) in Fig. 12B can be marking patterns as well because there are no distinctions between vias (1200) and vias (602). For example, all of the vias (602, 1200) have the same shape and size. See e.g., Figs. 12A and 12B of Wang. Thus, all of the circles (602, 1200) are marking patterns and all of the rectangles (1100, 700) are dummy patterns. Then, in Fig. 12 of Wang, the pad (600) includes more circles (602, 1200) than rectangles (1100, 700). For example, there are twenty six (26) circles and sixteen (16) rectangles. As such, in contrast to the Examiner's assertion, in Wang, a number of marking patterns (i.e., twenty six) is greater than a number of dummy patterns (i.e., sixteen). See e.g., Fig. 12B of Wang.

b. The Examiner has failed to show that Wang discloses marking patterns surrounding at least a group of dummy patterns as claimed in claim 23

In the October 11, 2007 Final Office Action, the Examiner states that Wang teaches dummy patterns (1200) and marking patterns (700). See October 11, 2007 Final Office Action,

Page 3. In stark contrast to the Examiner's assertion, elements (1200) are not dummy patterns for a CMP method formed in a uniform pattern over the semiconductor substrate. As discussed above, the elements (1200) are vias. The present application discloses that "as is well-known in the art, dummy patterns are intended to reduce dishing in a CMP process by reducing differences in pattern density." See page 2, lines 9-10 of the present application. As such, vias (1200) cannot be used to reduce dishing in a CMP process because vias are empty bores. Accordingly, in contrast to the Examiner's assertion, element 1200 cannot be a dummy pattern.

Furthermore, even assuming, *arguendo*, that the vias (1200) were dummy patterns, the patterns (700) do not surround a group of the vias (1200). In contrast, only a single via (1200) is surrounded by the patterns (700). See e.g., Fig. 12B of Wang.

c. The Examiner has failed to show that Wang discloses marking patterns and the predetermined plural numbers of the dummy patterns grouped by the marking patterns form a unit, which is repeated as claimed in claim 24

In the October 11, 2007 Final Office Action, the Examiner states that Wang teaches dummy patterns (700) and marking patterns (1200) wherein the marking patterns and the predetermined plural number of the dummy patterns grouped by the marking patterns form a unit, which is repeated (Fig. 12B, in one example the marking patterns (1200) can be grouped with the outside corner dummy patterns 700). See October 11, 2007 Final Office Action, Pages 3 and 4. As above, elements (1200) are not marking patterns, but vias. The vias form plugs when filled with a metal layer in a subsequent process. See e.g., paragraph [0075] of Wang. As such, the vias (1200) cannot be marking patterns used for counting the dummy patterns because the vias (1200) are hidden when filled with the metal layer.

Furthermore, even assuming, *arguendo*, that elements (1200) were marking patterns, Wang does not disclose that the dummy patterns (700) form a unit, much less a unit which is repeated. The Examiner states that the marking patterns (1200) can be grouped with the outside corner dummy patterns (700). However, it is not clear what the outside corner dummy pattern represents. Furthermore, none of the combination between the vias (1200) and the dummy patterns (700) repeat itself. See e.g., Fig. 12B of Wang.

d. The Examiner has failed to show that Wang discloses dummy patterns formed in a uniform pattern over the semiconductor substrate as claimed in claims 1, 23 and 24

In the October 11, 2007 Final Office Action, the Examiner states that Wang teaches dummy patterns (700) formed in a uniform pattern over the semiconductor substrate (Fig. 12B, 700 and paragraph 7). See October 11, 2007 Final Office Action, Page 2. However, the dummy patterns (700) in Fig. 12B of Wang are not formed uniformly over the semiconductor substrate. In contrast, the dummy patterns (700) have different sizes in that the dummy patterns (700) in the middle portions of the pad (600) are larger than other dummy patterns located around them. See Fig. 12B of Wang. Furthermore, the dummy patterns (700) are positioned in different directions. For example, some dummy patterns (700) are formed perpendicularly with respect to other dummy patterns (700). See Fig. 12B of Wang. As such, because the dummy patterns (700) are formed in different sizes and are positioned in different directions, the dumpy patterns (700) of Wang are not formed uniformly as claimed in claims 1, 23 and 24 of the present application.

For at least the above reasons, Applicants respectfully submit that claims 1, 23 and 24 and the claims dependent thereon are not anticipated by Wang.

Accordingly, for at least the above reasons, there are clear errors in the Examiner's rejections of claims 1-4, 23 and 24 under 35 U.S.C. § 102(e).

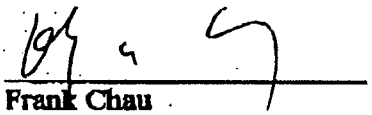
As such, Appellants respectfully submit that claims 1-4, 23 and 24 are not anticipated by Wang, and request that the Board reverse the Examiner's rejections of claims 1-4, 23 and 24 under 35 U.S.C. §102(e).

B. CONCLUSION

Accordingly, for at least the reasons set forth above, claims 1-4, 23 and 24 are believed to be in condition for allowance.

Therefore, it is respectfully requested that the Board reverse all claim rejections under 35 U.S.C. § 102.

Respectfully submitted,



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CLAIMS APPENDIX

1. A semiconductor device comprising:

a semiconductor substrate;

dummy patterns for a chemical mechanical polishing (CMP) method formed in a uniform pattern over the semiconductor substrate; and

marking patterns that are formed over the semiconductor substrate to correspond to predetermined groups of the dummy patterns,

wherein at least one dummy pattern is formed between two marking patterns, wherein a number of the dummy patterns is substantially greater than a number of the marking patterns.

2. The semiconductor device of claim 1, wherein the marking patterns have a different shape from the dummy patterns.

3. The semiconductor device of claim 1, wherein the marking patterns have a different size from the dummy patterns.

4. The semiconductor device of claim 1, wherein the marking patterns are smaller than the dummy patterns.

23. A semiconductor device comprising:

a semiconductor substrate;

dummy patterns for a chemical mechanical polishing (CMP) method formed in a uniform pattern over the semiconductor substrate; and

marking patterns that are formed over the semiconductor substrate to correspond to predetermined groups of the dummy patterns,

wherein the marking patterns surround at least a group of dummy patterns, wherein a size of the marking patterns is smaller than a size of the dummy patterns.

24. A semiconductor device comprising:

a semiconductor substrate;

dummy patterns for a chemical mechanical polishing (CMP) method formed in a uniform pattern over the semiconductor substrate; and

marking patterns that group predetermined plural numbers of the dummy patterns and are formed over the semiconductor substrate;

wherein the marking patterns and the predetermined plural numbers of the dummy patterns grouped by the marking patterns form a unit, which is repeated.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.